Patent Application
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SUBSTITUTE SPECIFICATION

RADIO FREQUENCY DEVICE WITH NULL OR QUASI-NULL INTERMEDIATE FREQUENCY MINIMIZING INTERFERING FREQUENCY MODULATION APPLIED TO AN INTEGRATED LOCAL OSCILLATOR

PRIORITY CLAIM

The present application is a 35 U.S.C. 371 filing from PCT/FR2003/002956 which is an international filing from French Application for Patent No. 02 12743, filed October 14, 2002, the disclosures of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[1] The present invention relates to the synthesis of frequency and more particularly to that utilized in radio frequency devices, receivers or transmitters, of the type with a null or quasi-null intermediate

frequency.

[2] The invention applies advantageously, but not with limitation, to wireless communication systems, and more particularly to cellular mobile telephones.

Description of Related Art

[3] In a terminal of a wireless communication system, such as for example a cellular mobile telephone, direct conversion, or transposition with null intermediate frequency, is an alternative to the superheterodyne architecture. Such conversion is particularly well adapted to allow architectural solutions which are very strongly integrated.

[4] A direct-conversion receiver, or else a receiver with null intermediate frequency (receiver zero-IF), converts the useful signal band directly around the null frequency (base band) instead of converting it to an intermediate frequency of the order of a few hundred MHz.

[5] A direct-conversion transmitter converts the base band of the signal directly around the radio frequency carrier frequency.

[6] In this case, zero-IF radio frequency devices have difficulty in differentiating the useful signal if continuous parasite signals are present at entry. Also, in certain cases, it is preferred to utilize radio frequency devices with quasi-null (low IF) intermediate frequency, that is, whereof the intermediate frequency is not strictly null, rather it is low and in practice

lower than one MHz.

[7] Regardless, to generate a useful or quasi-null intermediate frequency it is necessary to use a local oscillator frequency, or transposition frequency, close to the radio frequency to either cause frequency transposition towards the radio frequency field of the signal to be transmitted (in the case of a transmitter), or to cause frequency transposition downwards, of the signal received (in the case of a receiver).

[8] For the purposes of generating this transposition signal, a synthesizer having a frequency operating at a multiple frequency of the transposition frequency is generally used. And the transposition signal is then generated as it leaves a divider of suitable frequency.

[9] The frequency synthesizer is generally obtained with a voltage-controlled oscillator (VCO) and a phase locked loop (PLL).

[10] Due to imperfections in the chain of transmission or reception, parasite signals (harmonics or mixing products of useful signals) will exist and will be injected via parasite paths (magnetic coupling, capacitive coupling, and the like) in the voltage-controlled oscillator. The result is a frequency parasite modulation which is applied to the voltage-controlled oscillator. This mechanism is known to the expert as VCO PULLING.

[11] More precisely, when a parasite signal at a

phase-shifted Δf frequency relative to the output frequency of the local oscillator is applied to a voltage-controlled oscillator and operating at a given output frequency, this oscillator will be modulated in frequency with a frequency equal to Δf and an amplitude proportional to $1/\Delta f$. Furthermore, in devices of null or quasi-null intermediate frequency, Δf is low, resulting in increased amplitude.

[12] The result of this will be a perturbation in modulation at the output of the frequency transposition device or mixer, which is going to lead to more difficult decoding of information, and consequently to a more significant error rate.

[13] The effects of these parasite perturbations are modified due to the local oscillator belonging to a phase locked loop.

[14] More precisely, with respect to the phase locked loop, when the oscillator is modulated with a Δf frequency, the output of the charging pump of the phase locked loop is a sinusoidal wave having the Δf frequency. If Δf is greater than the cut-off frequency of the phase locked loop, the voltage control of the oscillator will not be affected. On the contrary, if Δf is low, that is, less than the cut-off frequency of the phase locked loop, the voltage control of the oscillator will act to reduce the amplitude of the modulation of the oscillator.

[15] Furthermore, since the oscillator is connected

to the phase locked loop, this results in a combination of two effects. Accordingly, at low frequency, the phase locked loop will correct perturbation. At high frequency, perturbation will be weak, due to the $1/\Delta f$ effect. On the contrary, in the vicinity of the cut-off frequency of the phase locked loop, there will be an increase in perturbation.

[16] A natural solution to this problem would consist of creating a phase locked loop having an elevated cut-off frequency.

[17] However, creating an increased cut-off frequency works against the stability of the loop. In effect, it is generally required, for reasons of stability, that this cut-off frequency is less than a tenth of the reference frequency of the loop.

[18] Now, when the loop creates an entire division in frequency, the reference frequency provides spacing between the channels. Thus, for DCS application in which the channels are spaced every 200 kHz in the 1808 MHz-1880 MHz range, the reference frequency is in practice equal to 400 kHz for an oscillator supplying a frequency of 3.6 Ghz.

[19] If the division made in the loop is not a whole division, then a higher reference frequency can be selected. However, using an improper divider is disadvantageous with respect to noise.

[20] All things considered, in a DCS application a loop cut-off frequency of the order of 40 to 50 kHz

maximum will be selected, which is largely insufficient to prevent the parasite problems of modulation mentioned above.

[21] Other solutions can be envisaged to rectify these problems of parasite modulation.

[22] Increased intermediate transposition frequencies, of the order of several MHz, can be used. However, this leads to an increase in current consumption of the receiver or transmitter.

[23] An oscillator supplying an output frequency which is an increased multiple of the required transposition frequency can also be used. But, this will have an impact on current consumption and will necessitate use of particularly complex technology.

[24] Finally, an attempt can be made to improve the insulation of the oscillator. But, this is particularly delicate to do on a chip, in particular when the chip also incorporates the frequency transposition means (or mixer).

[25] There is accordingly a need in the art to provide a more satisfactory solution to the problems of frequency parasite modulation applied to the oscillator, and quite particularly when this oscillator and the mixer are integrated on the same chip.

SUMMARY OF THE INVENTION

[26] The invention proposes a radio frequency device of the type with null or quasi-null intermediate

frequency, which is intended to receive or transmit a radio frequency signal whereof the transmission or reception frequency belongs to a frequency range subdivided into frequency channels.

[27] According to a general characteristic of the invention the radio frequency device, consequently capable of being a radio frequency receiver or a radio frequency transmitter, a means of frequency transposition is connected to a so-called main local oscillator on an integrated circuit chip.

[28] The main oscillator is incorporated within a main phase locked loop having a reference frequency supplied by a voltage-controlled auxiliary oscillator. The voltage controlled auxiliary oscillator is incorporated within an auxiliary phase locked loop having a reference frequency that is less than the frequency of the auxiliary oscillator.

[29] Furthermore, the reference frequency of the main loop, that is, the frequency of the auxiliary oscillator, is less than the output frequency of the main oscillator. It is furthermore greater than ten times the frequency spacing of the channels reduced to the output frequency of the main oscillator. In addition, this reference frequency of the main loop is removed by a whole multiple of the send or receive frequency of at least the cut-off frequency of the main loop.

[30] In other words, the invention proposes a

frequency synthesizer with double phase locked loop.

[31] A first oscillator, an auxiliary oscillator, allows all the desired characteristics for the transposition signal (channel selection, stability, phase noise, etc.) to be attained. This oscillator is controlled by the auxiliary loop. As this auxiliary oscillator oscillates at a frequency which does not correspond to any harmonic nor produce a mix of useful signals, it will not be perturbed.

[32] A second oscillator, a main oscillator, oscillating for example at twice the transposition frequency, will be controlled by the main loop in taking the output frequency of the oscillator auxiliary as reference. As the reference frequency of the main loop is relatively high, the loop filter can have a relatively wide pass-band, of the order of several tens of MHz, having the following advantages:

all the interference will be reduced by the loop gain, and

the phase noise of the main oscillator will be directly given by the noise of the auxiliary oscillator.

[33] As a consequence, it is not necessary to provide a high-performance oscillator, as a simple ring oscillator will be adequate.

[34] When the auxiliary loop is intended for use with a whole divider, the reference frequency of the auxiliary loop is less than or equal to, preferably equal to, the frequency spacing of the channels reduced

to the reference frequency of the main loop.

[35] Furthermore, according to an embodiment of the invention, the reference frequency of the main loop is greater than the a twentieth of the output frequency of the main oscillator.

[36] Therefore, in an embodiment in which the range of frequencies to which the send or receive frequency belongs is in the vicinity of 900 MHz or 1800 MHz (corresponding to the GSM or DCS standard), the reference frequency of the main loop can be taken as equal to 450 MHz, whereas the reference frequency of the auxiliary loop can be equal to 50 kHz. The output frequency of the main oscillator can then be equal to 3.6 Ghz.

[37] The electronic integrated circuit chip, which already comprises the frequency transposition means as well as the local main oscillator, may also comprise the two phase locked loops.

[38] Moreover, the device can be integrally produced on the electronic chip.

[39] The invention also proposes a component of a wireless communications system, for example a cellular mobile telephone, incorporating a radio frequency device, such as defined above.

BRIEF DESCRIPTION OF THE DRAWINGS

[40] A more complete understanding of the method and apparatus of the present invention may be acquired

by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[41] FIGURE 1 diagrammatically illustrates a cellular mobile telephone incorporating in its transmission chain a frequency synthesizer according to the present invention;

[42] FIGURE 2 diagrammatically illustrates a cellular mobile telephone incorporating in its reception chain a frequency synthesizer according to the present invention; and

[43] FIGURE 3 illustrates in greater detail, though still diagrammatically, an embodiment of a synthesizer according to the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[44] In FIGURE 1, the reference TP designates a cellular mobile telephone intended in this example to function according to the DCS standard. In the DCS standard, the transmission frequency of the radio frequency signal or the reception frequency is part of a frequency range of between 1808 MHz and 1880 MHz, this frequency range being subdivided into frequency channels spaced at 200 kHz.

[45] A voltage-controlled oscillator, to be designated hereinafter as "main oscillator," bears the reference VCOP and emits an output signal SSP at an output frequency here equal to 3.6 Ghz. This main VCOP

oscillator is followed by a frequency divider by two oscillators, designated as DV, supplying a transposition signal ST at a frequency of 1.8 Ghz.

[46] A complex mixer MX (that is, processing the two channels I and Q, in phase and quadrature) receives, on the one hand, the transposition signal ST and, on the other hand, a useful signal in base band SUBB delivered by the processor in base band PBB of the telephone TP. At the mixer output the signal is modulated around the frequency of 1.8 MHz and is then transmitted by the antenna ANT of the telephone after passing into a preamplification stage PPA followed by a power amplification stage PA.

[47] In the reception chain of the telephone TP, such as illustrated in FIGURE 2, and connected to the output chain by a duplexer not shown here, the signal received by the antenna ANT is amplified in a low-noise amplifier LNA. Next, the signal is transposed in base band through the mixer MX by using the frequency transposition signal ST, likewise originating from a VCOP oscillator.

[48] The useful signal in base band SUBB is then supplied after amplification and numerical analog conversion to the processor in base band PBB of the telephone TP.

[49] One skilled in the art will note that the architecture described here for the chain of transmission or reception of the telephone TP is a so-

called "zero IF" architecture, that is, with a null intermediate frequency.

[50] Notwithstanding the foregoing, the invention also applies to radio frequency receivers or radio frequency transmitters of the type having a quasi-null intermediate frequency, that is, for example less than 1 MHz.

[51] In high-integration solutions, as are currently recommended, the frequency transposition stage (or mixer) and the main oscillator VCOP are situated on the same electronic integrated circuit chip PC.

[52] Due to imperfections in the send or receive chain, parasite signals (frequency harmonics or mixing products of useful signals) will appear and will be injected via parasite paths into the main oscillator, resulting in frequency parasite modulation applied to this main oscillator, and known to those skilled in the art by the name of "VCO PULLING."

[53] The present invention provides a solution to this problem, particularly critical when the main oscillator VCOP and the mixer MX are on the same integrated circuit chip PC.

[54] The present invention proposes a frequency synthesizer having two phase locked loops PLL1 and PLL2, such as shown in FIGURE 3.

[55] More precisely, the main oscillator VCOP is incorporated into a "main" phase locked loop, and designated as PLL2. This phase locked loop

conventionally comprises a front detector PFD2 followed by a charging pump CP2 and a loop filter FB2. The output of the loop filter controls the voltage oscillator VCOP. The oscillator output VCOP supplies the signal SSP, and the output signal is also divided by a whole number k2 using a whole divisor DV2 before being compared to a reference signal SRFP in the front detector PFD2.

[56] The reference signal SRFP is delivered by a another (auxiliary) voltage-controlled oscillator VCOA, itself incorporated into an auxiliary phase locked loop designated as PLL1. The architecture of this loop PLL1 is similar to that of the loop PLL2, with the difference that the whole division is this time carried out by divisor DV1 using a whole number k1.

[57] Furthermore, the reference signal SRFA of the loop PLL1 is supplied by an external generator, for example a quartz oscillator.

[58] In general, the frequency of the reference signal SRFP must be large to have a sufficiently wide band-pass of the loop PLL2, typically greater than 1 MHz, and in such a way that the loop PLL2 sharply reduces the effect of PULLING to which the oscillator VCOP is subject.

[59] Furthermore, the frequency of the reference signal SRFP must be in a non-contaminated zone, that is, it must be removed by a whole multiple of the transmit or receive frequency, by at least the cut-off frequency

of the main loop.

[60] Accordingly, by way of example, for a telephone operating according to the DCS standard, a frequency of 450 MHz for the signal SRFP can be selected. The cut-off frequency of the loop can then be selected up to 1/10 of the frequency of the signal SRFP, here 45 MHz. In this case the choice will be guided by criteria peculiar to the application (noise, consumption, and the like).

[61] Furthermore, since the frequency spacing of the channels is 200 kHz for an output receiving frequency in the vicinity of 1.8 GHz (corresponding to frequency spacing of 400 kHz for a frequency of the signal SSP equal to 3.6 GHz, or else to spacing of 50 kHz for the frequency of 450 MHz of the signal SRFP), a frequency of 50 kHz for the reference signal SRFA will be selected.

[62] Thus, the reference frequency of the auxiliary loop is equal to the frequency spacing of the channels, reduced to the reference frequency of the main loop.

[63] Since the oscillator VCOA oscillates at a frequency in a non-contaminated zone, that is, not corresponding to any harmonic nor produced from a mix of useful signals, it will not be perturbed.

[64] Furthermore, although the main oscillator VCOP is subject to PULLING, the effect will be strongly reduced by the loop gain of the loop PLL2.

[65] Although preferred embodiments of the method

and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.